Overview of NEMSIC project: low power integrated sensing with Nano-Electro-Mechanical devices

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Outline

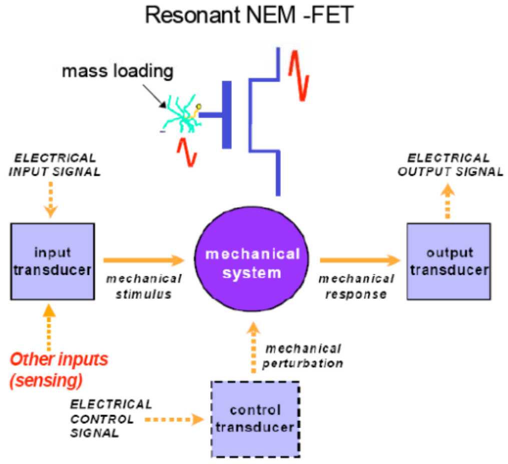
- Objectives, partnership and ambition.
- Technology and devices:
  - Thin film SOI NEMS resonators for integrated low power sensing.
  - Functionalization of silicon-based sensors.
  - Power management with NEM-FETs.
- Technical progress: status and highlights.
- Conclusions and perspectives

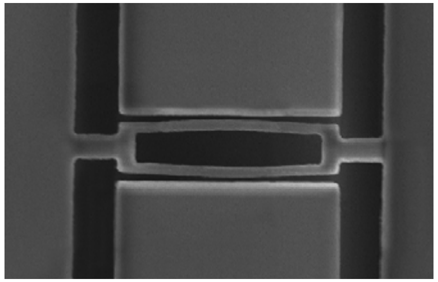
NEMSIC objectives

Hybrid Nano-Electro-Mechanical / Integrated Circuit Systems for Sensing and Power Management

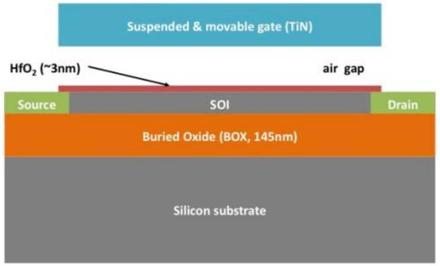
- Technological objectives
- Sensor and device objectives
- NEM-CMOS application objectives

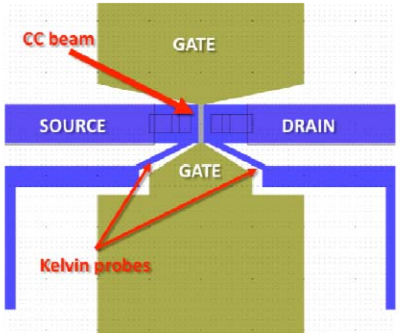
1. Resonant sensor.





2. Power management switch.





Technological objectives

- **TO1**: Development and validation of a NEM) technology platform for both sensing and power management applications, at CEA-LETI.
- **TO2**: Combination of NEM silicon nanowires device with CMOS in true hybrid technological demonstrators.
- **TO3**: Fast prototyping for Movable-Gate FET operated in power management applications.
- **TO4**: Technology for functionalized layers and their integration on the NEM technology platform on movable NEM gate or insulator levels, dedicated to gas and bio-molecule sensing.

Sensor objectives

- **SDO1:** Design and fabrication of dedicated NEM sensors for gas sensing based on vibrating structures able to push the sensitivity to extreme values.
- **SDO2:** Design and fabrication of dedicated Bio-NEM sensors.
- **SDO3:** Design and fabrication of power management (sleep transistor) NEM-FET switch.

System objectives

- **SYSO1:** Realization of a full hybrid sensor/CMOS interface low power smart sensor systems exploiting NEM resonant arrays for gas (COx, NOx, SOx) sensing.
- **SYSO2:** Realization and experimental validation of a Bio-NEMS system for real-time measurements of analytes such as DNA or proteins.
- **SYSO3:** Experimental benchmarking of power savings at circuit and system level by use sleep NEM-FET transistor with reliable operation.

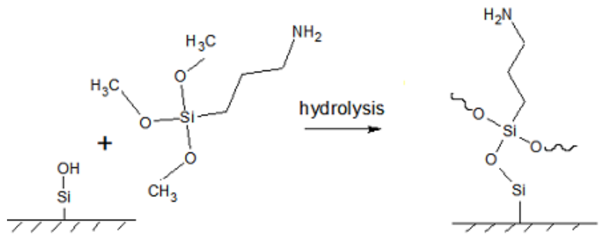
Partnership

- **EPFL**, Switzerland
- **TUD**, The Netherlands
- **IMEC-NL**, The Netherlands
- **SOU**, United Kingdom
- **CEA-LETI**, France
- **SCIPROM**, Switzerland
- **IMEC**, Belgium
- **HON**, Romania
- **UNIGE**, Switzerland - replaced by **HiQScreen.**

WP1: highlights

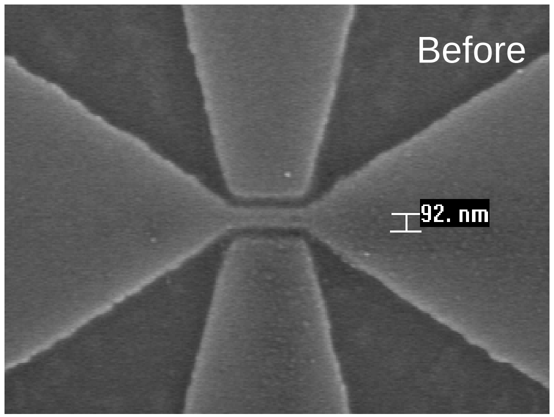
- **Effects of functionalisation on the conductance of SiNW sensor devices (SOU, IMEC-BE)**

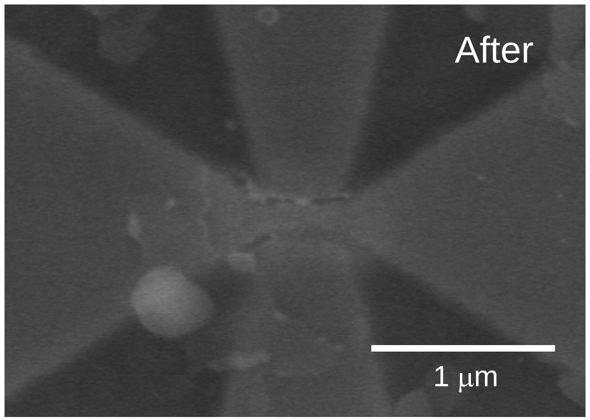
NH_2 Self-assembled Monolayer (NH_2 SAM) + Glutaraldehyde(GA) + Biotin

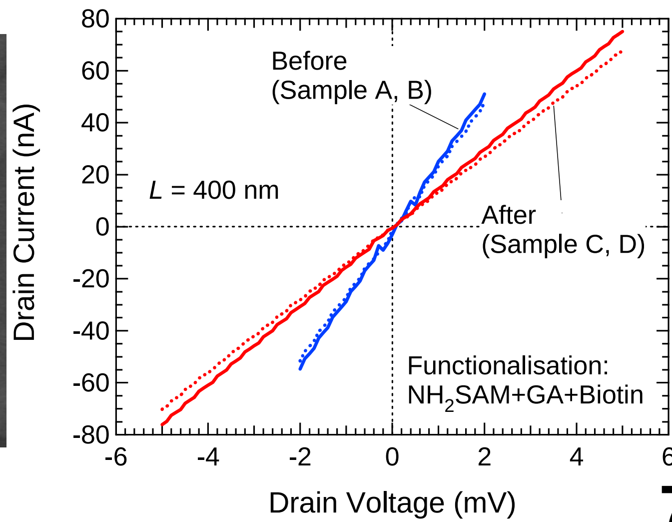


NH_2 SAM coating

Functionalisation: conductance decreased

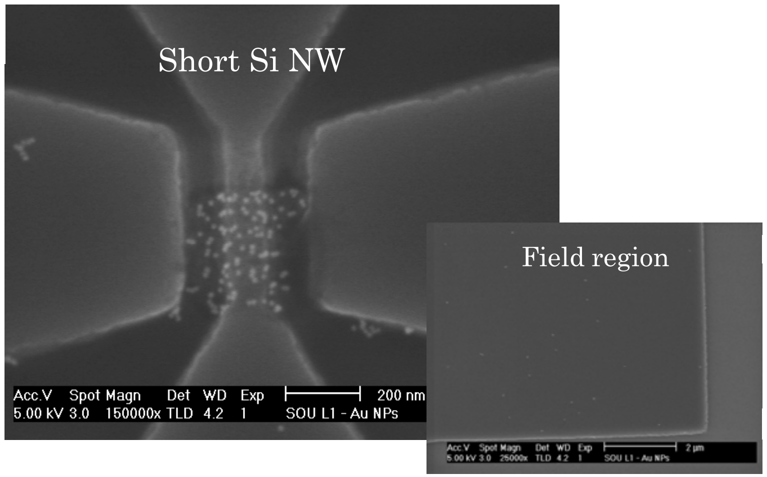


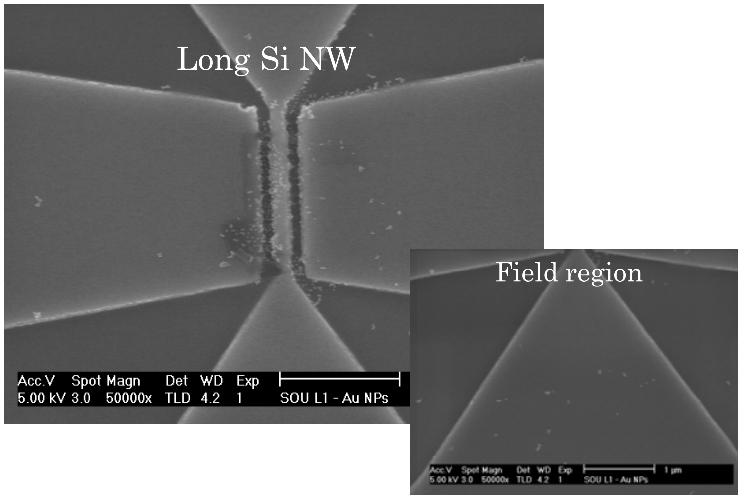




WP1: highlights

- **Development of selective functionalisation technology on SiNW devices:**
  - o Functionalisation on SiO_2 surface for bio-sensing (IMEC-BE)
  - o Functionalisation on Si-H surface for gas sensing (IMEC-NL)



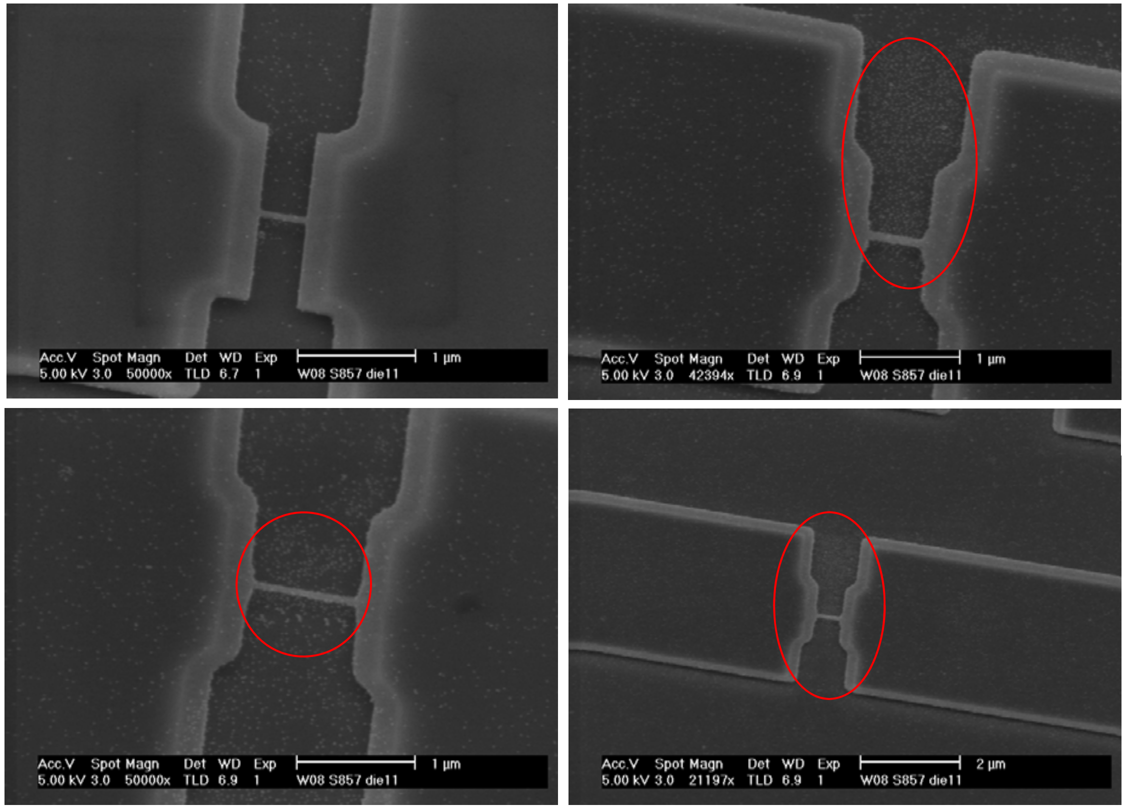


- Only NWs were decorated by Au NPs (15 nm)
- Amino functionality is only on the NWs

S. Armini., Invited Talk at Annual Meeting of COST Action MP0802

WP1: highlights

- **Selective surface functionalization on <u>suspended</u> Si NWs (IMEC-NL, CEA-LETI, SOU)**

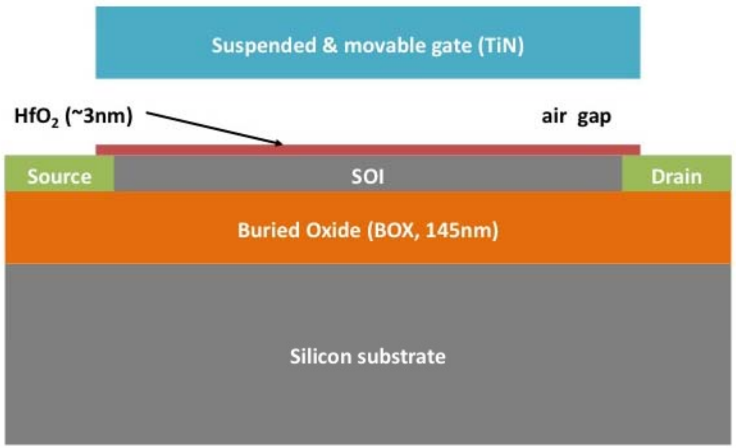


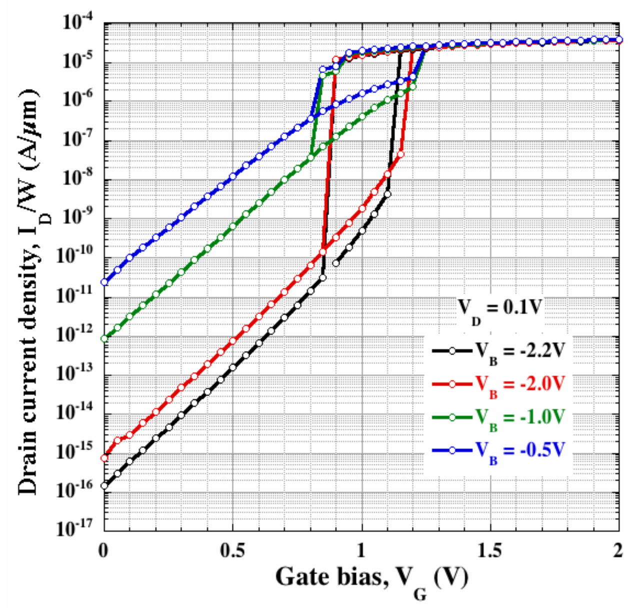
SEM characterization of the Si NWs after ebeam selective NH_2SAMs functionalization followed by Au NPs decoration of the NH_2 groups.

WP2: highlights

- Hybrid FEA based optimization of FD SOI NEMFET: feedback to fabrication platform and tapeout by EPFL.

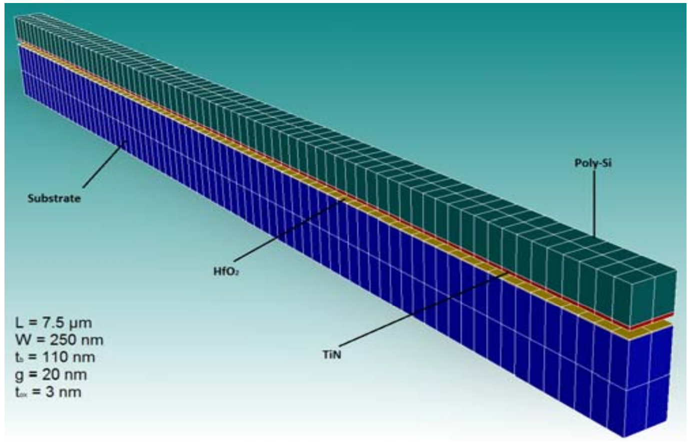
	symbol	Min. Value	Target	Max. Value	Unit
SOI thickness	t_{SOI}		30		nm
Buried Oxide thickness (BOX)	t_{BOX}		145		nm
HfO_2 thickness	t_{ox}		3		nm
Gap	g	10		50	nm
Gate length – beam width	$L_{ch}=w_{beam}$	150		600	
Beam length	l_{beam}	150		50000	nm
Gate thickness (TiN+poly-Si)	t_{gate}		110		nm
Beam anchors minimum dimensions			2		µm

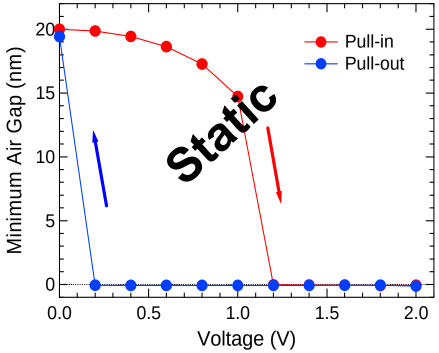


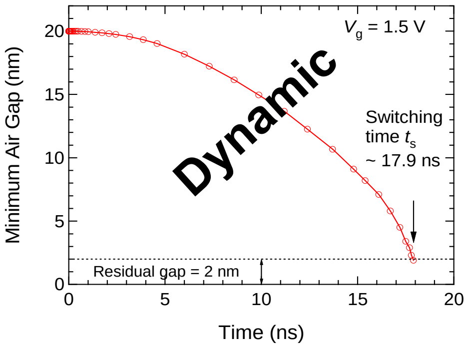


WP2: highlights

- Implementation of the compact model for the **Fully Depleted SOI NEMFET based on the Berkeley's BSIM Independent Multiple Gate (IMG)** compact model for double-gate (independent gate) devices.
- Complete parameter extraction of the FD NEMFET compact model performed for a complete design space exploration.
- First version of the Agilent ADS Design Kit (DK) based on the Verilog-A compact model for FD SOI NEMFET was released







WP2: highlights

Power components, energy and the energy-delay product for 3 major design implementations:

- **Reference**
- **Hybrid**
- **Leakage-enhanced**

NEMFET low leakage power offers a 2.75x advantage in the OFF power over the classic high-VT transistors.

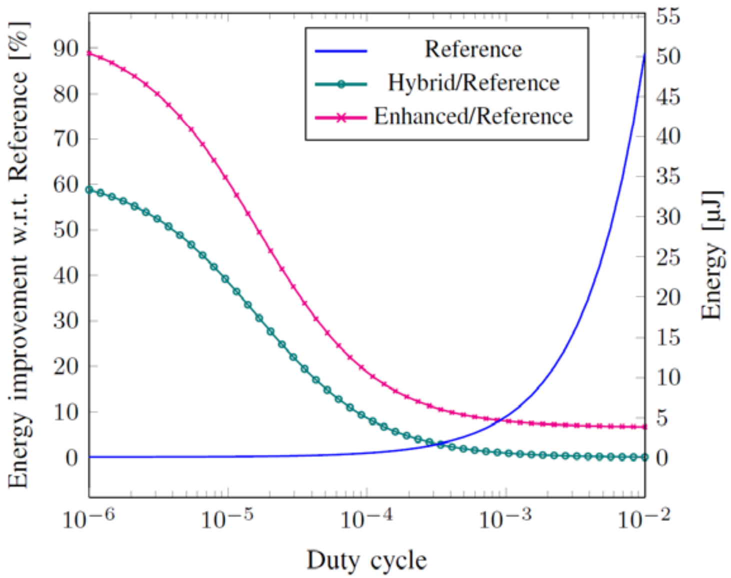


Table 1 – Power, energy and energy-delay results

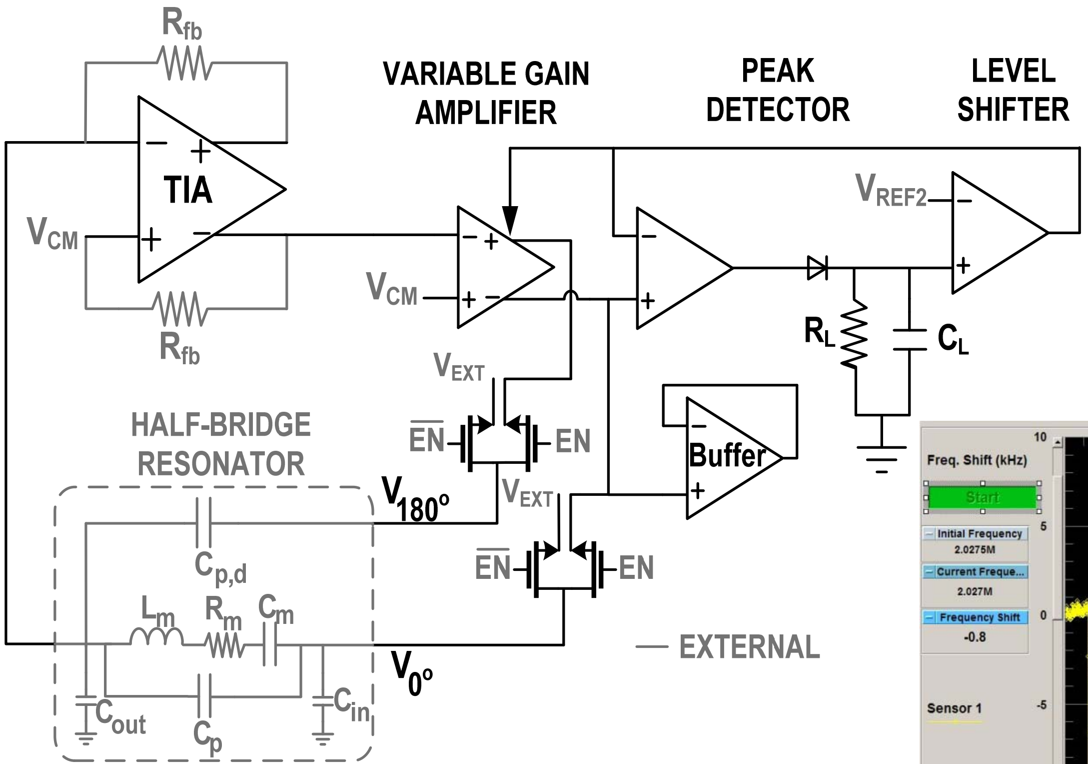
Implementation type	ON power [mW]	OFF power [nW] STs	OFF power [nW] Always-on cells	OFF power [nW] Total	Power-up energy [pJ]	Total energy [μJ]	Energy-Delay Product [μJ·ns]
Reference	5.0340	56.28	26.02	81.28	48.04	9.05	62.01
Hybrid	5.0339	4.52	26.02	29.52	37	8.61	56.47
Leakage-Enhanced	4.7	4.52	0.364	4.884	37	8	51.48

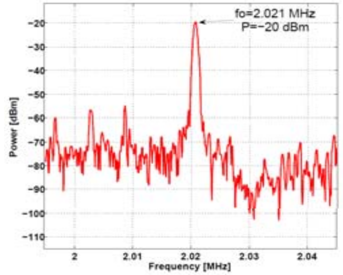
Active time = 1.73 ms, Idle time = 993.35 ms, Transition time = 5.32 ms @ 150 MHz

Always-on cells = Power management controller and isolation cells

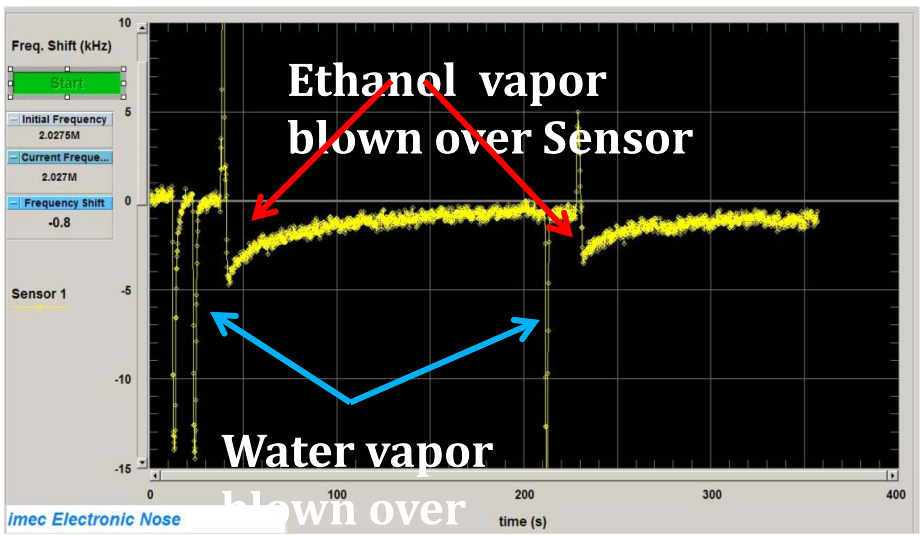
WP3: highlights

2MHz MEMS Oscillator design and validation (IMEC-NL)



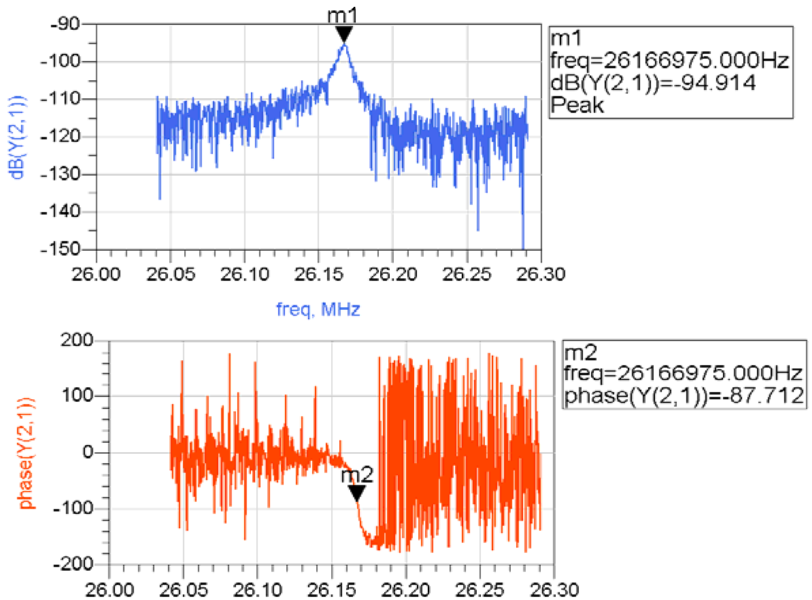


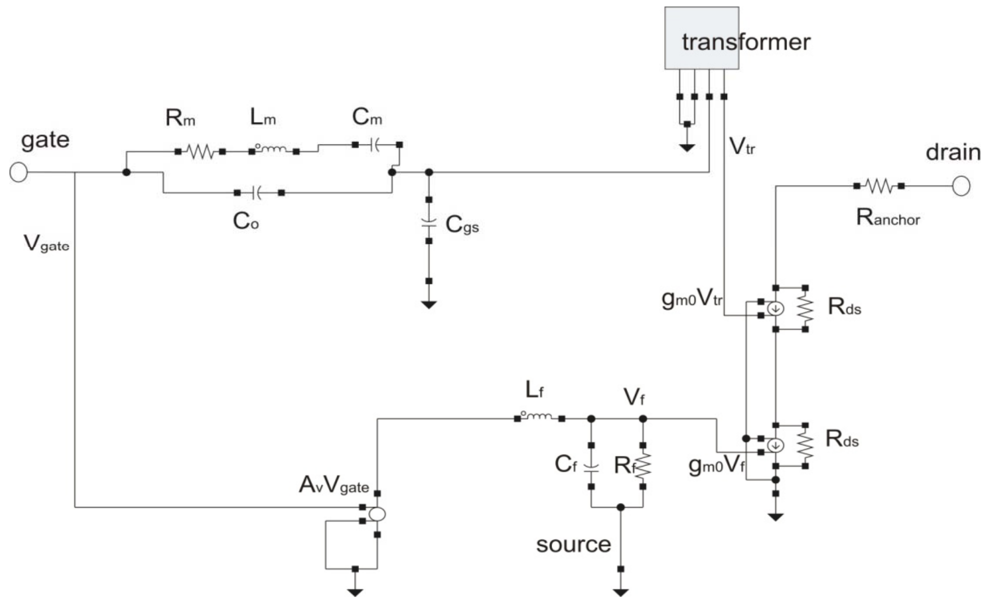
Operation as a sensor system proven



WP3: highlights

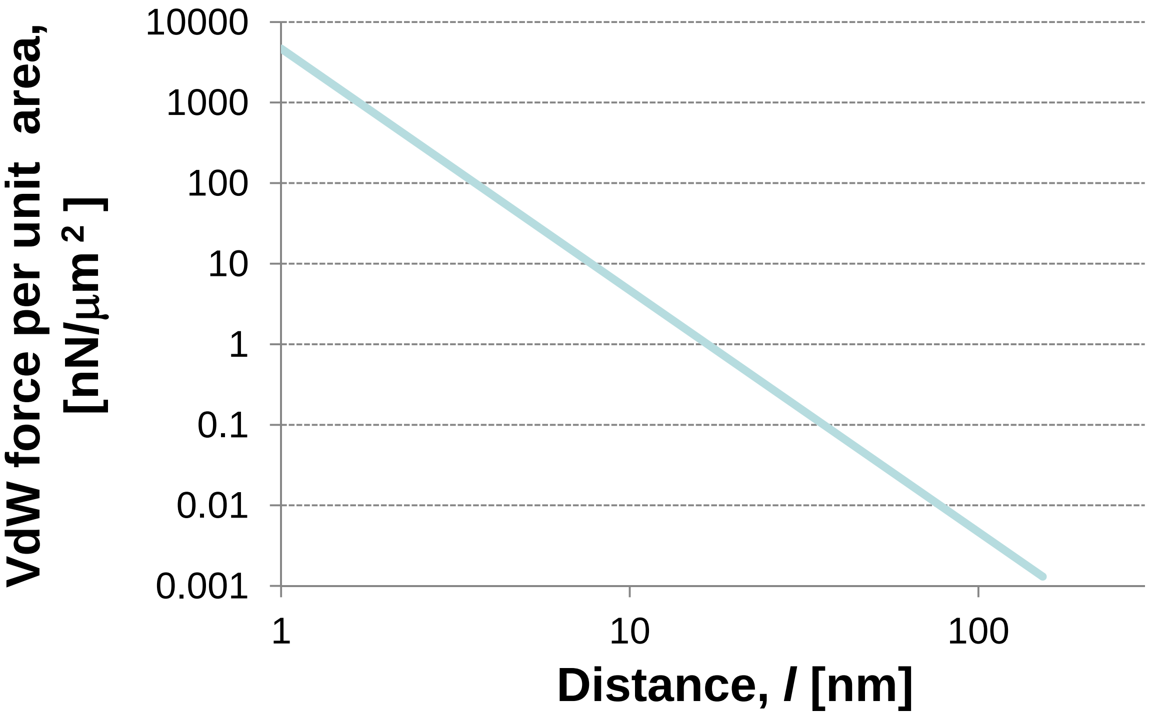
- VB-FET small signal model experimentally calibrated and specific features (phase shift and gain) captured in model (EPFL, IMEC-NL) able to serve CMOS-NEMS circuit design





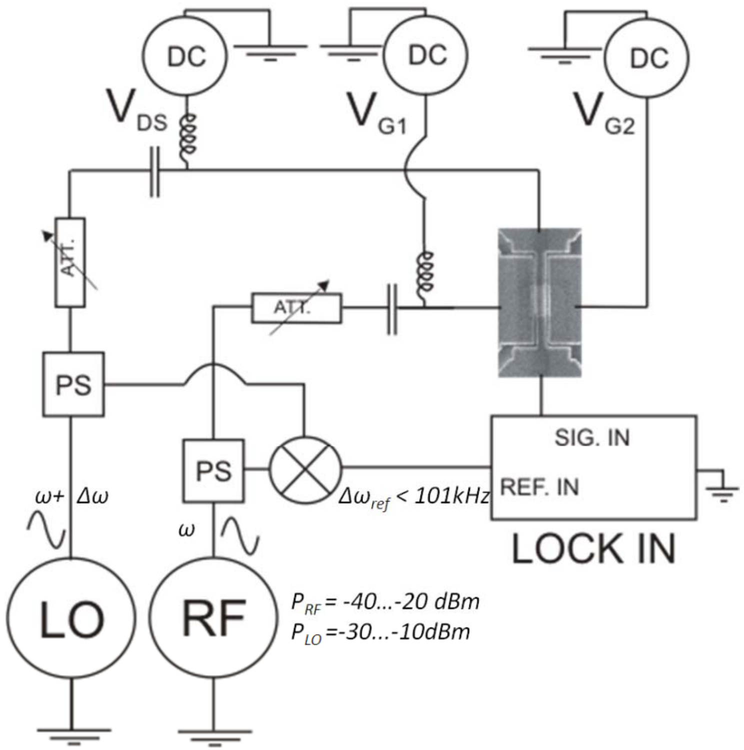
WP4: highlights

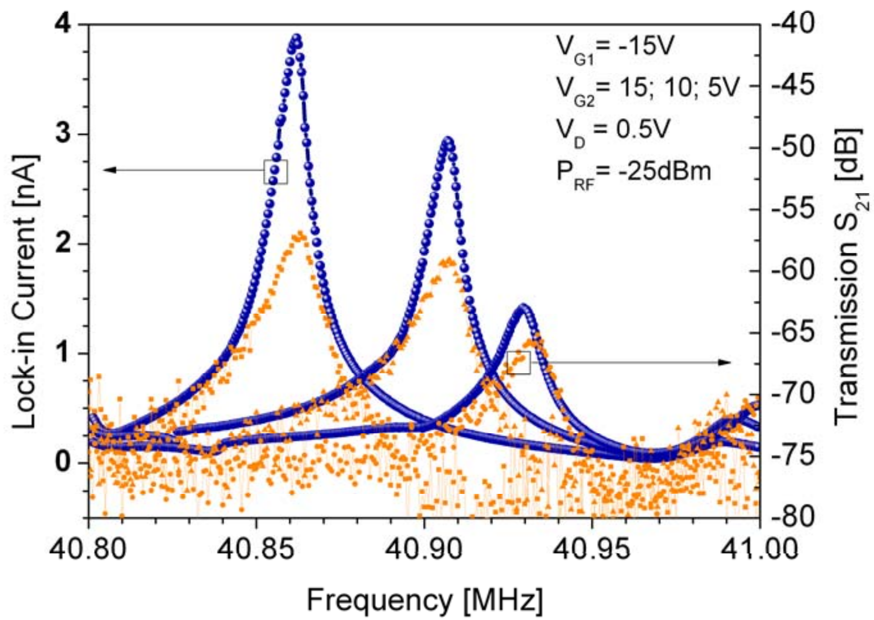
• Investigation by IMEC-BE of nanoscale forces relevant for the designed devices (SiO2 plates): VdW relevant.
• Compare with estimated electrostatic force/area in FD SOI NEMFETs: 0.03-0.3 nN/µm^2



WP4: highlights

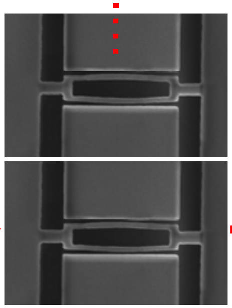
- Successful mixer lock-in amplifier measurement setup by EPFL to avoid the effect of parasitic feedthrough capacitance, enabling high frequency measurements in vibrating nanostructures.





Highlight WP4 & demo: RF front-end receiver based on RB- FinFETs

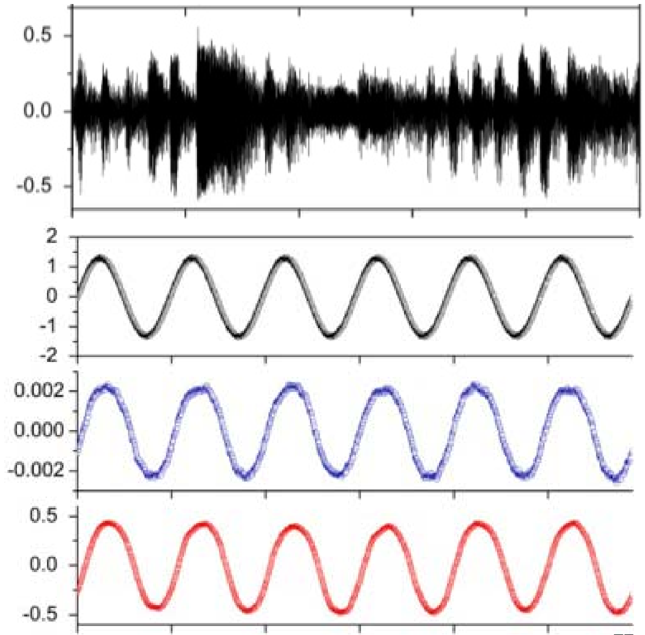
Carrier (AM/FM/digital/…)



recovered signal

ALL-IN-ONE:
channel selection, demodulation & filtering by array of FinFET resonators

Demodulation example

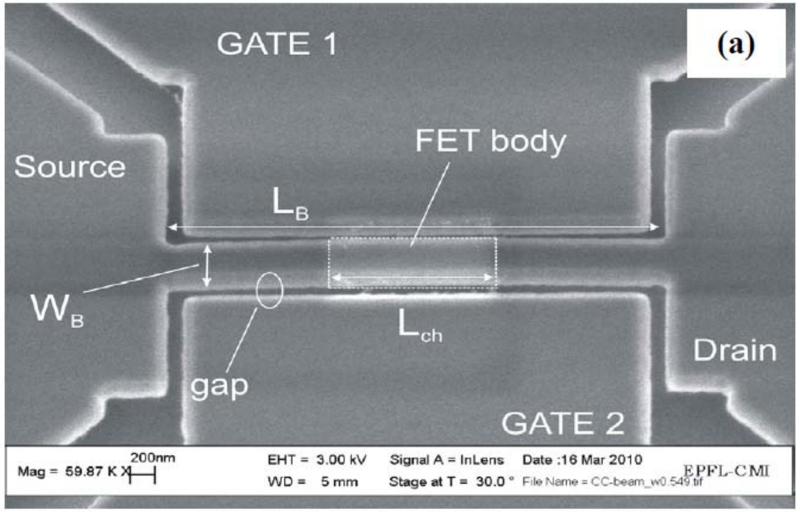


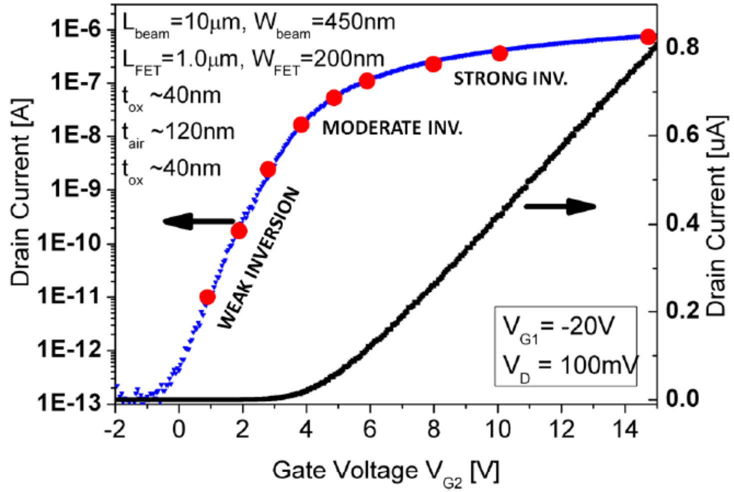
Frequency selective demodulation of audio signal using the array of RB-FinFETs is successfully demonstrated

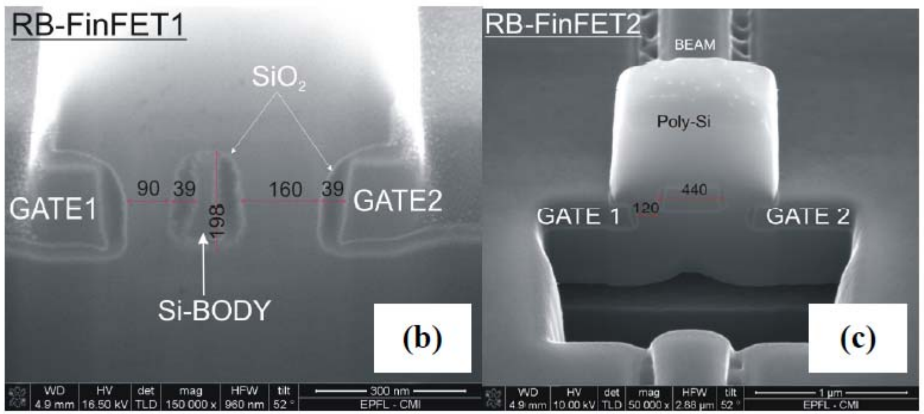
This work is submitted to ISSCC 2012

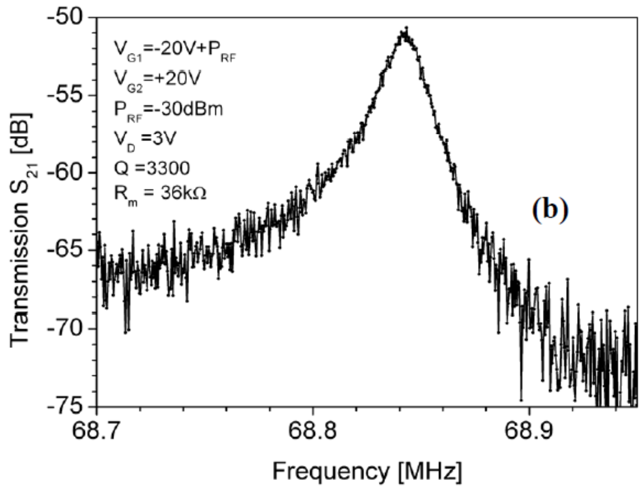
WP5: highlights - prototyping

Vibrating body FET of EPFL operating from weak to strong inversion with sub-nW power consumption demonstrated and reported at IEDM 2010.









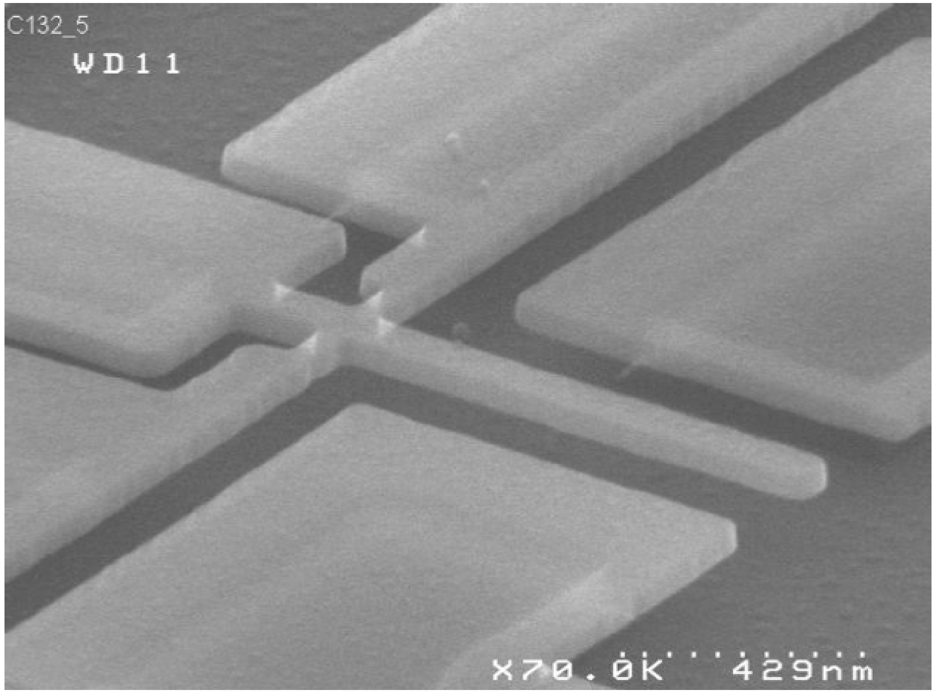
WP5: highlights – techno platform

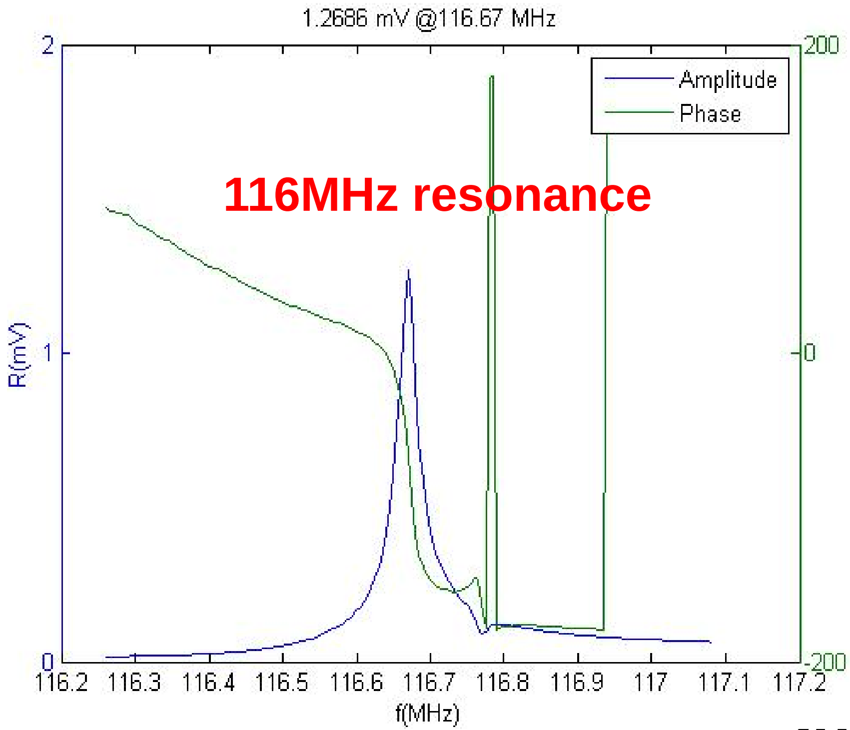
Technology platform for NEMS-CMOS devices @ CEA-LETI:

- **Finalization of NEMS device fabrication on both sensor and power management platforms**: no further delay in the project due to highly prioritized technology processing at LETI, in line with the new DOW.
- **Compatibility with CMOS ICs fully proven experimentally**
- **High frequency resonator sensors functional in various designs: publications to follow!**
- NEM-FET switch fabricated, basic functionality but high leakage, characterization work in progress

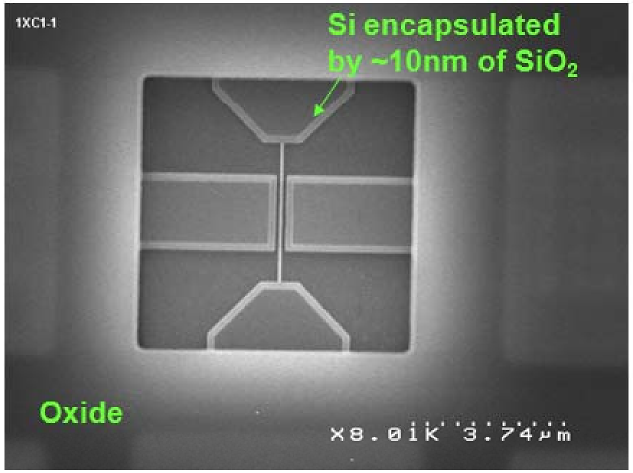
WP5: highlights

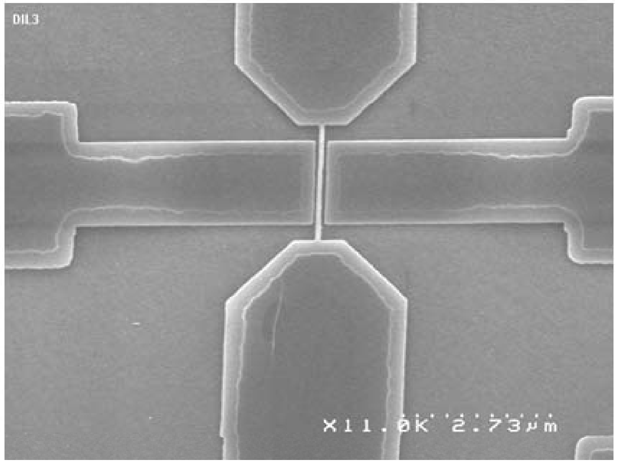
- Fully functional NEM resonators: cross-beam (CEA-LETI).
- Also experimental demonstrator at the 3rd review.





WP5: highlights Y3





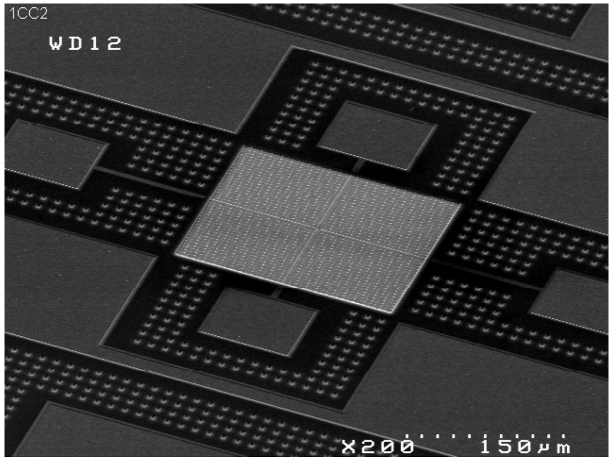
Fabricated designs:

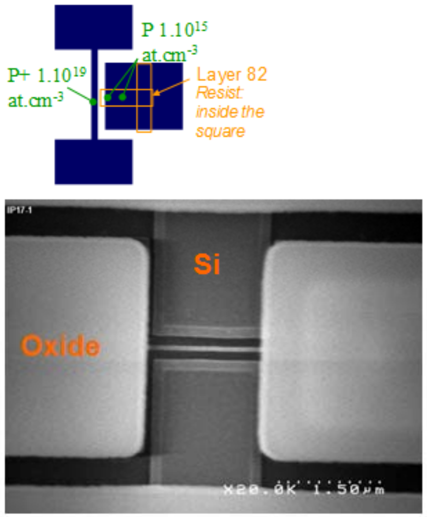
- EPFL
- SOU

Collaborative design platform implemented by CEA-LETI

Vibrating Body FET (VBFET)

Vi





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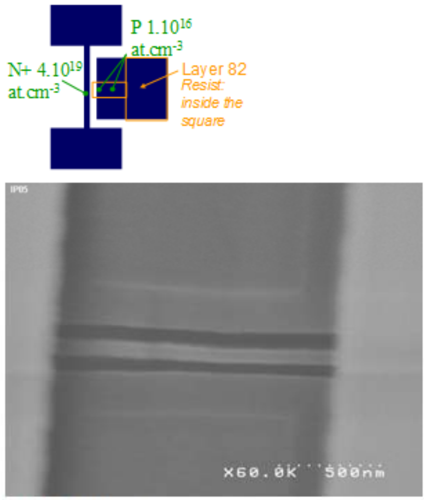

LSGFET

Conclusion and Roadmap

• The NEMSIC project made significant progress towards both low power integrated sensing and power management objectives

• NEMSIC contributed to establish a new application roadmap for integrated NEM sensors and power management.